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Alexandria, VA 22313-1450

From: Pamela J. Squyres
Attorney Docket: MA-068
Phone: 408-869-2921

FAX NUMBER 571-273-8300

Re: Patent Application of: Maitreyee Mahajani et al.	Examiner: Thao X. Le
Serial No.: 10/079,472	Group Art Unit: 2814
Filed: February 19, 2002	Attorney Docket No.: MA-068
Title: Gate Dielectric Structures for Integrated Circuits and Methods for Making and Using Such Gate Dielectric Structures	

Document(s) Transmitted:

- Reply Brief (7 pages)
- Exhibit A (3 pages)

Total pages of this transmission, including the cover letter: 11
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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

In re patent application of
Maitreyee Mahajani et al.

Attorney Docket No. MA-068

Serial No. 10/079,472

Group Art Unit: 2814

Filed: February 19, 2002

Examiner: Thao X. Le

For: GATE DIELECTRIC STRUCTURES FOR INTEGRATED CIRCUITS AND METHODS FOR MAKING AND USING SUCH GATE DIELECTRIC STRUCTURES

REPLY BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

April 12, 2006

To the Commissioner:

The above-captioned case is under appeal. Appellant respectfully files this Reply Brief in response to the Examiner's Answer mailed on February 14, 2006. An Appendix listing the pending claims is included in this Reply Brief.

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Pamela J. Squyres, Reg. no. 52,246

4/13/06
Date of Deposit

SUMMARY

The following discussion responds to the Examiner's Answer. Rebuttal is made to points raised by the Examiner in his Response to Argument, beginning at paragraph 10 on page 6. In the interest of brevity, Appellant has limited rebuttal to new points raised in the Examiner's Answer. Where Appellant believes the Examiner's arguments to have been sufficiently addressed by the Appeal Brief, those arguments will be allowed to stand and will not be repeated.

DISCUSSION

This Discussion will identify points in the Response to Argument section of the Examiner's Answer that require rebuttal, then will provide such rebuttal.

- **Page 7, paragraph beginning "Issue A ..."**

The Examiner argues that a contiguous stack is not recited in the claims. Appellant concedes that the words "contiguous stack" in fact do not appear in the claims. But Appellant respectfully points out that these claims recite forming a channel region, forming a first oxide on the channel region, forming a nitride layer on the first oxide layer, and forming a second oxide layer on the nitride layer. It will be apparent that if each layer is formed on the one before it, a contiguous stack will necessarily be created.

- **Page 9, line beginning "Third, the interpretation ..."**

The Examiner suggests:

> "... the interpretation of the word 'polysilicon' would simply mean that 'many or more than one silicon elements or atoms'. Such 'polysilicon' layer or substrate may have different crystal orientation structure and the claim language has failed to identify the crystal structure of the substrate. Thus, the Examiner submits that the silicon substrate 16 of Halliyal would comprise multiple silicon atoms or elements bonding together forming a 'polysilicon substrate' and would read on the claim limitation."

Appellant notes that the word "polysilicon" has not been coined by Appellant, but is a well-known term of art. The Examiner is correct that (as noted at the bottom of page 8 of the Answer) silicon has three usual forms: monocrystal, polycrystal, and amorphous. Monocrystalline silicon is a single silicon crystal, with no grain boundaries. Silicon wafers are formed of monocrystalline silicon. Polycrystalline silicon, a term typically shortened to

polysilicon, consists of multiple silicon grains. Amorphous silicon has no crystalline structure. To give just one example, Exhibit A includes a typical definition from www.semiconfareast.com, which begins "Thin films of polycrystalline silicon, or **polysilicon** ..." (emphasis original.)

Appellant believes the Examiner to be suggesting that the term "polysilicon" can be interpreted to mean "many silicon atoms", regardless of crystalline structure, and thus that the monocrystalline channel region 16, because it contains many silicon atoms, can be considered to be polysilicon. Appellant will respectfully maintain that such an interpretation is contrary to well-established usage, and that the term "polysilicon" will be understood by those skilled in the art to refer to polycrystalline silicon.

Appellant believes the remainder of the Examiner's arguments have largely been addressed either in the Appeal Brief or in this Reply Brief and thus will not repeat them here.

CONCLUSION

Appellant respectfully solicits the Honorable Board of Patent Appeals and Interferences to reverse the rejections of the pending claims and pass this application on to allowance.

Respectfully submitted,

4/13/06
Date

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APPENDIX

1-8. (Cancelled or withdrawn)

9. A method for making a SONOS device, comprising:

providing a channel region;

providing a first oxide layer on the channel region by an in-situ steam generation process;

providing a silicon nitride layer on the first oxide layer; and

providing a second oxide layer on the silicon nitride layer, wherein the device is a SONOS device.

10-11. (Cancelled)

12. The method of claim 9, wherein the in-situ steam generation process is performed at a temperature ranging from about 750 to about 1050 degrees Celsius.

13. The method of claim 9, wherein the in-situ steam generation process is performed at a pressure ranging from about 100 millitorr to about 760 torr.

14. The method of claim 9, wherein the in-situ steam generation process is performed for a time sufficient to deposit an oxide thickness of about 10 to about 200 angstroms.

15. The method of claim 9, further including annealing the oxide layer in a nitric oxide atmosphere.

16-23. (Cancelled or withdrawn)

24. A SONOS semiconductor device made by a method comprising:

providing a channel region;

providing a first oxide layer on the channel region by an in-situ steam generation process;

providing a silicon nitride layer on the first oxide layer; and

providing a second oxide layer on the silicon nitride layer wherein the device is a SONOS semiconductor device.

25. (Withdrawn)

26. An integrated circuit containing a SONOS semiconductor device made by a method comprising:

providing a polysilicon layer;

providing a first oxide layer on the polysilicon layer by an in-situ steam generation process;

providing a silicon nitride layer on the first oxide layer; and

providing a second oxide layer on the silicon nitride layer wherein the device is a SONOS semiconductor device.

27-35. (Cancelled or withdrawn)

36. A method for making a SONOS device, comprising:

providing a polysilicon channel region;

providing a first oxide layer in contact with the polysilicon channel region by an in-situ steam generation process;

providing a silicon nitride layer in contact with the first oxide layer; and

providing a second oxide layer in contact with the silicon nitride layer.

37. A SONOS semiconductor device made by a method comprising:

providing a polysilicon channel region;

providing a first oxide layer in contact with the polysilicon channel region by an in-situ steam generation process;

providing a silicon nitride layer in contact with the first oxide layer; and

providing a second oxide layer in contact with the silicon nitride layer.

38. An integrated circuit containing a SONOS semiconductor device made by a method comprising:

providing a polysilicon layer;

providing a first oxide layer in contact with the polysilicon layer by an in-situ steam generation process;

providing a silicon nitride layer in contact with the first oxide layer; and

providing a second oxide layer in contact with the silicon nitride layer, wherein the device is a SONOS semiconductor device.

39-42. (Cancelled or withdrawn)

Exhibit A

Wafer Fab Links:

Incoming Wafers
Epitaxy
Diffusion
Ion Implant
Polysilicon
Dielectric
Lithography/Etch
Thin Films
Metallization
Glassivation
Probe/Trim

See Also:

Polysilicon Deposition
Semicon Manufacturing
Wafer Fab Equipment

Wafer Fab: Polysilicon

Thin films of polycrystalline silicon, or **polysilicon** (also known as poly-Si or poly), are widely used as MOS transistor gate electrodes and for interconnection in MOS circuits. It is also used as resistor, as well as in ensuring ohmic contacts for shallow junctions. When used as gate electrode, a metal (such as tungsten) or metal silicide (such as tantalum silicide) may be deposited over it to enhance its conductivity.

Poly-Si is known to be compatible with high temperature processing and interfaces very well with thermal SiO2. As a gate electrode, it has also been proven to be more reliable than Al. It can also be deposited conformally over steep topography. Heavily-doped poly thin films can also be used in emitter structures in bipolar circuits. Lightly-doped poly films can also be used as resistors.

Poly-Si is usually deposited by thermal decomposition or pyrolysis of silane at temperatures from 580-650 degrees C, with the deposition rate exponentially increasing with temperature. The deposition rate is also affected by the pressure of silane, which translates to silane concentration. Other important variables in polysilicon deposition are pressure and dopant concentration.

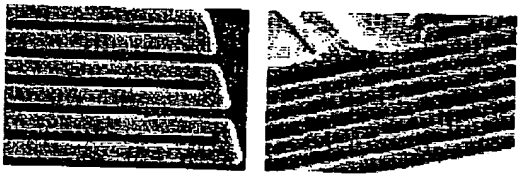

Fig. 1. SEM Photos of Polysilicon Lines

The electrical characteristics of a poly-Si thin film depends on its doping. As in single-crystal silicon, heavier doping results in lower resistivity. Poly-Si is more resistive than single-crystal silicon for any given level of doping mainly because the grain boundaries in poly-Si hamper carrier mobility. Common dopants for polysilicon include arsenic, phosphorus, and boron. Polysilicon is usually deposited undoped, with the dopants just introduced later on after deposition.

There are three ways to dope polysilicon, namely, diffusion, ion implantation, and in situ doping. Diffusion doping consists of depositing a very heavily-doped silicon glass over the undoped polysilicon. This glass will serve as the source of dopant for the poly-Si. Dopant diffusion takes place at a high temperature, i.e., 900-1000 deg C. Ion implant is more precise in terms of dopant concentration control and consists of directly bombarding the poly-Si layer with high-energy ions. In situ doping consists of adding dopant gases to the CVD reactant gases during the epi deposition process.

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Fig. 2. Example of a Low-Pressure CVD (LPCVD) furnace that can be used for polysilicon deposition

See also: Polysilicon Deposition; Polysilicon Doping

BOOKS on POLYSILICON for SALE at Amazon.com:

1) Polycrystalline Silicon for Integrated Circuits and Displays
2) Polysilicon Thin Films and Interfaces: Symposium Held April 17-19, 1990, San Francisco, California, U.S.A. (Materials Research Society Symposium Pro)
3) Polysilicon Films and Interfaces (Materials Research Society Symposium Proceedings, Vol 106)

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